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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/775,677	CHA ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6-19,21-23,25-27 and 59-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2, 3, 6-8, 13-16, 18, 19, 22, 25-27 and 59-75* is/are rejected.

7)☒ Claim(s) *4,9-12,17,21 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed September 1, 2005.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 59-75 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 2, lines 2-3 recites the limitation of "a raised pattern on the substrate wherein the raised pattern has a surface opposite the substrate". Claim 2, lines 17-18 recites the limitation of "wherein the raised pattern comprises a trench isolation pattern in the semiconductor substrate". It is unclear how the raised pattern can have a surface that is "opposite the substrate" when the entire raised pattern is, in fact, a part of the substrate itself. Therefore, the metes and bounds of claims 2 and 59-75, which depend upon claim 2, cannot be determined.

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2, 63, 64 and 71-75 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato et al. (US 6,798,038, previously cited).

Regarding claim 2, Sato discloses a substrate (1) and a raised pattern on the substrate, forming a first insulating layer (2/12/6/7) on the raised pattern and on the substrate wherein

forming the first insulating layer comprises forming a first portion (2/12) of the first insulating layer on the surface of the raised pattern opposite the substrate and on the substrate using a first processing condition and forming a second portion (6/7) of the first insulating layer on the surface of the raised pattern opposite the substrate and on the substrate using a second processing condition so that the first portion is between the second portion and the surface of the raised pattern opposite the substrate, after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate, and after removing portions of the first insulating layer, forming a second insulating layer (8) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (Fig. 4A-4H; col. 6, ln. 30 – col. 7, ln. 18). Sato discloses that the substrate is a semiconductor substrate, wherein the raised pattern is a trench isolation pattern in the semiconductor substrate and wherein maintaining portions of the first insulating layer on the substrate includes maintaining portions of the first insulating layer in trenches defined by the trench isolation pattern (Fig. 4A-4H; col. 6, ln. 30 – col. 7, ln. 18).

Regarding claim 63, Sato discloses that the first portion of the first insulating layer is on the surface of the raised pattern opposite the substrate and in the trenches defined by the trench isolation pattern (Fig. 4B; col. 6, ln. 30 – col. 7, ln. 18).

Regarding claim 64, Sato discloses that the first portion of the first insulating layer is between the second portion of the first insulating layer and the trenches defined by the trench isolation pattern (Fig. 4B; col. 6, ln. 30 – col. 7, ln. 18).

Regarding claim 71, Sato discloses that forming the first insulating layer includes forming the first insulating layer using HDP-CVD (col. 6, ln. 36-37).

Regarding claim 72, Sato discloses removing portions of the first insulating layer by etching back portions of the first insulating layer without mechanical polishing by etching back (col. 6, ln. 36-38; col. 4, ln. 42-49).

Regarding claim 73, Sato discloses removing portions of the first insulating layer by mechanical polishing separate from etching back (col. 6, ln. 52-56).

Regarding claim 74, Sato discloses removing portions of the first insulating layer beyond portions of the raised pattern so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern (Fig. 4C).

Regarding claim 75, Sato discloses that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer (Fig. 4B).

Claims 3, 6-8, 15, 16, 18, 19, 22 and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al. (US 6,204,161, previously cited).

Regarding claim 6, Chung discloses a substrate (100) and a raised pattern (250/260) on the substrate, forming a first insulating layer (300) on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion of the first insulating layer using a first processing condition and forming a second portion (300) of the first insulating layer using a second processing condition, after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the

raised pattern while maintaining portions of the first insulating layer on the substrate, and after removing portions of the first insulating layer, forming a second insulating layer (340/360) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (col. 7, ln. 38 – col. 8, ln. 36). Chung discloses that the first insulating layer includes closed voids therein, and removing portions of the first insulating layer includes opening the voids in the first insulating layer (Fig. 4B; col. 7, ln. 60 – col. 8, ln. 7). Figure 4B-4C of Chung shows forming openings in the voids such that the widest part of the void is exposed.

Regarding claim 3, Chung discloses that the substrate is an integrated circuit substrate, the raised pattern is a pattern of transistor gate electrodes, and maintaining portions of the first insulating layer on the substrate includes maintaining portions of the first insulating layer between transistor gate electrodes (col. 5, ln. 64 – col. 6, ln. 16).

Regarding claims 7 and 26, Chung discloses that the closed voids are located in the first insulating layer between portions of the raised pattern.

Regarding claims 8 and 27, Chung discloses that the second insulating layer fills the opened voids (col. 8, ln. 25-36).

Regarding claim 15, Chung discloses forming the first insulating layer using a high density plasma chemical vapor deposition (HDP-CVD) (col. 7, ln. 45-59).

Regarding claims 16 and 22, Chung discloses that removing portions of the first insulating layer involves etching back portions of the first insulating layer without mechanical polishing while etching back (col. 7, ln. 66 – col. 8, ln. 24).

Regarding claim 18, Chung discloses that removing portions of the first insulating layer involves removing portions of the first insulating layer beyond portions of the raised pattern so

that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern (Fig. 4C).

Regarding claim 19, Chung discloses that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer (Fig. 4B).

Regarding claim 25, Chung discloses a substrate (100) and a raised pattern (250/260) on the substrate, forming a first insulating layer (300) on the raised pattern and on the substrate wherein the height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern, after forming the first insulating layer, removing portions of the first insulating layer while maintaining portions of the first insulating layer so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed between portions of the raised pattern, and after removing portions of the first insulating layer, forming a second insulating layer (340/360) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (col. 7, ln. 38 – col. 8, ln. 36). Chung discloses that the first insulating layer includes closed voids therein, and removing portions of the first insulating layer includes opening the voids in the first insulating layer (Fig. 4B; col. 7, ln. 60 – col. 8, ln. 7). Figure 4B-4C of Chung shows forming openings in the voids such that the widest part of the void is exposed.

Claims 2, 6-8, 16, 18, 19, 22, 25-27, 59-64, 72, 74 and 75 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (US 6,150,238, cited in IDS).

Regarding claim 2, Wu discloses a substrate (100) and a raised pattern on the substrate, forming a first insulating layer (104a/108a) on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion (104a) of the first insulating layer on the surface of the raised pattern opposite the substrate and on the substrate using a first processing condition and forming a second portion (108a) of the first insulating layer on the surface of the raised pattern opposite the substrate and on the substrate using a second processing condition so that the first portion is between the second portion and the surface of the raised pattern opposite the substrate, after forming the first insulating layer including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate, and after removing portions of the first insulating layer, forming a second insulating layer (112) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (Fig. 2B-2G; col. 2, ln. 41 – col. 3, ln. 9). Wu discloses that the substrate is a semiconductor substrate, wherein the raised pattern is a trench isolation pattern in the semiconductor substrate and wherein maintaining portions of the first insulating layer on the substrate includes maintaining portions of the first insulating layer in trenches defined by the trench isolation pattern (Fig. 2B-2G; col. 2, ln. 41 – col. 3, ln. 9).

Regarding claim 6, Wu discloses a substrate (100) and a raised pattern on the substrate, forming a first insulating layer (104a/108a) on the raised pattern and on the substrate wherein forming the first insulating layer comprises forming a first portion (104a) of the first insulating layer using a first processing condition and forming a second portion (108a) of the first insulating layer using a second processing condition, after forming the first insulating layer

including the first and second portions, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate, and after removing portions of the first insulating layer, forming a second insulating layer (112) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (col. 2, ln. 41 – col. 3, ln. 9). Wu discloses that the first insulating layer includes closed voids therein, and removing portions of the first insulating layer includes opening the voids in the first insulating layer (col. 2, ln. 55-66). Figure 2D-2E of Wu shows forming openings in the voids such that the widest part of the void is exposed.

Regarding claims 7, 26 and 61, Wu discloses that the closed voids are located in the first insulating layer between portions of the raised pattern.

Regarding claims 8, 27 and 62, Wu discloses that the second insulating layer fills the opened voids (col. 2, ln. 55-66).

Regarding claims 16, 22 and 72, Wu discloses that removing portions of the first insulating layer involves etching back portions of the first insulating layer without mechanical polishing while etching back (col. 2, ln. 55-64).

Regarding claim 18, Wu discloses that removing portions of the first insulating layer involves removing portions of the first insulating layer beyond portions of the raised pattern so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern (Fig. 2E).

Regarding claim 19, Wu discloses that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer (Fig. 2D).

Regarding claim 25, Wu discloses a substrate (100) and a raised pattern on the substrate, forming a first insulating layer (104a/108a) on the raised pattern and on the substrate wherein the height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern, after forming the first insulating layer, removing portions of the first insulating layer while maintaining portions of the first insulating layer so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed between portions of the raised pattern, and after removing portions of the first insulating layer, forming a second insulating layer (112) on the exposed portions of the raised pattern and on the maintained portions of the first insulating layer (col. 2, ln. 41 – col. 3, ln. 9). Wu discloses that the first insulating layer includes closed voids therein, and removing portions of the first insulating layer includes opening the voids in the first insulating layer (col. 2, ln. 55–66). Figure 2D-2E of Chung shows forming openings in the voids such that the widest part of the void is exposed.

Regarding claim 59, Wu discloses that the first insulating layer includes closed voids therein and removing portion of the first insulating layer involves opening voids in the first insulating layer (col. 2, ln. 55-66).

Regarding claim 60, Wu discloses that the openings in the voids are substantially at least as wide as any portions of the opened voids between the opening and the substrate.

Regarding claim 63, Wu discloses that the first portion of the first insulating layer is on the surface of the raised pattern opposite the substrate and in the trenches defined by the trench isolation pattern (col. 2, ln. 41 – col. 3, ln. 9).

Regarding claim 64, Wu discloses that the first portion of the first insulating layer is between the second portion of the first insulating layer and the trenches defined by the trench isolation pattern (col. 2, ln. 41 – col. 3, ln. 9).

Regarding claim 74, Wu discloses removing portions of the first insulating layer beyond portions of the raised pattern so that the raised pattern extends beyond the maintained portions of the first insulating layer and so that the maintained portions of the first insulating layer are recessed relative to the exposed portions of the raised pattern (Fig. 2E).

Regarding claim 75, Wu discloses that a height of the first insulating layer between portions of the raised pattern is greater than a height of the raised pattern before removing portions of the first insulating layer (Fig. 2D).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US 6,204,161) in view of Papasouliotis et al. (US 6,030,881, previously cited).

Regarding claim 13, Chung discloses forming the second portion (300) of the first insulating layer by using a HDP-CVD process (col. 7, ln. 45-59). Chung does not specifically disclose the process conditions involved in these deposition processes. Like Chung, Papasouliotis discloses using an HDP-CVD process to deposit oxide materials between features

of an integrated circuit. Papasouliotis discloses that oxide material can be successfully HDP-CVD deposited using a pressure of 1.5-25 mTorr and a bias power of 500-10000 kW (Table 1). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the pressure and bias power taught by Papasouliotis when depositing the second portion of the first insulating layer of Chung because Chung discloses forming the layer by HDP-CVD but does not disclose any particular process conditions and Papasouliotis teaches that the process conditions that can be used to successfully deposit an oxide layer using HDP-CVD.

Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al. (US 6,798,038) in view of Papasouliotis et al. (US 6,030,881).

Regarding claim 69, Sato discloses forming the second portion (6/7) of the first insulating layer by using a HDP-CVD process (col. 11, ln. 45 – col. 13, ln. 48). Sato does not specifically disclose the process conditions involved in these deposition processes. Like Sato, Papasouliotis discloses using an HDP-CVD process to deposit oxide materials between features of an integrated circuit. Papasouliotis discloses that oxide material can be successfully HDP-CVD deposited using a pressure of 1.5-25 mTorr and a bias power of 500-10000 kW (Table 1). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the pressure and bias power taught by Papasouliotis when depositing the second portion of the first insulating layer of Sato because Sato discloses forming the layer by HDP-CVD but does not disclose any particular process conditions and Papasouliotis teaches that the process conditions that can be used to successfully deposit an oxide layer using HDP-CVD.

Regarding claim 70, Papasouliotis discloses that oxide material can be successfully HDP-CVD deposited using an oxygen gas flow rate of 10-1000 sccm, a helium gas flow rate of 10-1000 sccm and a silane gas flow rate of 10-250 sccm (Table 1).

Allowable Subject Matter

Claims 4, 9-12, 17, 21 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the indication of the allowable subject matter of claim 4 is the inclusion therein, in combination as currently claimed, of the limitation of forming first and second portions of a first insulating layer having closed voids on a pattern of bit lines, removing portions of the first insulating layer to expose portions of the bit lines while maintaining portions of the first insulating layer on the substrate, and forming a second insulating layer on the exposed portions of the bit lines. This limitation is found in claim 4 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reason for the indication of the allowable subject matter of claims 9 and 21 is the inclusion therein, in combination as currently claimed, of the limitation of a first portion of the first insulating layer using a first pressure and forming a second portion of the first insulating layer using a second pressure that is different from the first pressure such that the first insulating layer has closed voids. This limitation is found in claims 9 and 21 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reason for the indication of the allowable subject matter of claim 10 is the inclusion therein, in combination as currently claimed, of the limitation of forming a first portion

of the first insulating layer using a first bias power and forming a second portion of the first insulating layer using a second bias power that is different from the first bias power such that the first insulating layer has closed voids. This limitation is found in claim 10 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reason for the indication of the allowable subject matter of claim 11 is the inclusion therein, in combination as currently claimed, of the limitation of forming the first portion of the first insulating layer using a bias power, forming a second portion of the first insulating layer such that the first insulating layer has closed voids, and removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate. This limitation is found in claim 11 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reason for the indication of the allowable subject matter of claim 12 is the inclusion therein, in combination as currently claimed, of the limitation of forming first and second portions of a first insulating layer having closed voids on a raised pattern, removing portions of the first insulating layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate, and forming a second insulating layer on the exposed portions of the raised pattern, wherein the first portion of the first insulating layer is formed using a process gas of silane and oxygen. This limitation is found in claim 12 and is neither disclosed nor taught by the prior art of record, alone or in combination.

The primary reason for the indication of the allowable subject matter of claims 17 and 23 is the inclusion therein, in combination as currently claimed, of the limitation of forming a first insulating layer having closed voids on a raised pattern, removing portions of the first insulating

layer to expose portions of the raised pattern while maintaining portions of the first insulating layer on the substrate, and forming a second insulating layer on the exposed portions of the raised pattern, wherein the portions of the first insulating layer are removed by mechanical polishing. This limitation is found in claims 17 and 23 and is neither disclosed nor taught by the prior art of record, alone or in combination.

Response to Arguments

Applicant's arguments filed September 1, 2005 have been fully considered but they are not persuasive.

Regarding the rejection of claim 2 as being anticipated by Sato, Applicant argues that the oxide film 12 (first portion of the first insulating layer) is allegedly not between the HDP film 6/7 (second portion of the first insulating layer) and a surface of the raised pattern opposite the substrate. For the reasons stated above, the limitation of the raised pattern having "a surface opposite the substrate" when the raised pattern *is* the substrate is unclear and confusing. It is not understood to what "surface" this limitation refers. Figure 4B of Sato shows that the first portion of the first insulating layer (2/12) is between the second portion of the first insulating layer and the raised pattern of the substrate (6/7).

Regarding the rejection of claim 6 as being anticipated by Chung, Applicant argues that Chung allegedly fails to teach or suggest openings in voids that are at least as wide as any portions of the opened voids between the openings and the substrate. However, Figure 4C of Chung shows that the voids present as shown in Figure 4B have been completely opened.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
November 8, 2005

Michael Trinh
Primary Examiner